Electronic
components
and materials

PHILIPS

THE ABC ADAPTABLE BOARD COMPUTER SP55

AN APPLICATION MEMO

signetics

INTRODUCTION

System development cards are designed to simplify the user's task when doing microprocessor evaluation prototyping. To achieve this goal, the card should be designed with enough flexibility to make it adaptable to individual requirements. It should contain a certain amount of RAM for storage of programs under development. A ROM or PROM or a combination of both should be provided for permanent storage of programs such as debug software. The card should be designed for easy interfacing to current loop or RS-232 terminal devices. Buffers should be provided for address, data and control lines to facilitate expansion of memory and I/O logic. The use of one or more general-purpose ports will aid in I/O interfacing. In summary, the overall design philosophy should be to add nothing to the card that is not a basic necessity. This philosophy maximizes cost effectiveness and minimizes unused design features.

This applications memo describes the various components and applications of the ABC (Adaptable Board Computer) 1500 system development card. Topics covered include:

- ABC1500 memory organization
- Memory and I/O port decoding
- I/O interface
- Bus and control line buffers
- Clocking requirements
- Minimum ABC system configuration
- Addition of 1K of RAM memory
- Step mode operation
- Synchronous and asynchronous operation
- I/O port interface design examples
- Interrupt option
- Kit considerations
- Component identification list
- ABC1500 edge connector signal list

THE ABC1500

The objective of the ABC1500 card is to enable the user to develop 2650-based systems in a configuration that fits his particular needs. The card is designed around the Signetics 2650 8-bit microprocessor. It contains 1K bytes of ROM with the PIPBUG* debug program, 512 bytes of RAM, 2 general-purpose parallel I/O ports, 1 serial I/O port, and buffers for the address, data, and control lines.

Wire jumpers are included for selecting from among several available memory and I/O port configurations, terminal interface schemes, and operating modes. Additional circuitry can be added to the card in the wire-wrap area provided. Expansion of the card is made possible by feeding all buffered address, data and control lines into a 100-pin edge connector.

An assembly drawing and a logic diagram of the ABC1500 are shown in Figures 1 and 2, respectively.

If the current-loop interface is used, only a single 5 volt supply is necessary to power the entire card. When communicating with RS-232 type terminal devices, a ±12 volt power supply is also required.

The ABC card is sold either as a completely assembled and tested card (2650PC1500) or in kit form (2650KT9500).

*PIPBUG, a program debug module, is described in detail in Signetics MOS Microprocessor Applications Memo SS50.

ABC1500 MEMORY ORGANIZATION

To simplify memory decoding, a trade-off was made between usable memory space and the complexity of the decoder. By allocating the entire 8K of page zero to the on-card memory and limiting memory expansion to 24K (adequate for the majority of prototyping applications), considerable simplification was realized. Only 2, 16-pin ICs are required to perform both memory selection and I/O port decoding.

Three address lines (A9, A11, and A12) are not used to address the on-card memory. The result is that the on-card ROM and RAM appear to occupy the entire 8K page in an interweaving pattern as shown in Table 1. This prohibits external memory from using any of the page zero memory space, and the first allowable location for add-on memory is 2000_{16}, or the beginning of page 1. All of pages 1, 2 and 3 are available for memory expansion.

ROM Configuration

The 1K bytes of ROM are implemented with one 2608 NMOS static ROM (IC7) that contains PIPBUG, a firmware aid used to enter and debug user programs. Since the ROM occupies the first 1K bytes of address space, the 2650 will enter PIPBUG when the card is reset. If the debug program is not required, the ROM can be removed from its socket and replaced with a user ROM or with two 82S115 (512 x 8) PROMs, for which board space is provided (IC5 and IC6). However, the ROM and PROMs cannot be used together since they occupy the same address space.

RAM Configuration

The 512 bytes of RAM are implemented with four 2112-2 (256 x 4) NMOS static RAMs (ICs 1, 2, 3, 4). They are located in the memory address space from 400_{16} to $5FF_{16}$, but also appear to occupy other address spaces in page 0 as shown in Table I. Since the second block of memory occupies the "top" of page 0, the on-card RAM may be used to store indirect addresses or subroutines which can be accessed by the ZBRR and ZBSR instructions with negative offsets.

Since PIPBUG resides in the first 1K of memory, an interrupting device cannot use

ADDRESS LINES						DECIMAL ADDRESS	ORGANIZATION	HEX ADDRESS
A14	A13	A12	A11*	A10	A9**			
						8k		1FFF
0	0	X	X	1	X		SECOND BLOCK RAM	
							FIRST BLOCK RAM	
						7k	SECOND BLOCK RAM	1BFF
0	0	X	X	0	X		FIRST BLOCK RAM	
							PIPBUG ROM	
						6k		17FF
0	0	X	X	1	X		SECOND BLOCK RAM	
							FIRST BLOCK RAM	
						5k	SECOND BLOCK RAM	
0	0	X	X	0	X		FIRST BLOCK RAM	13FF
							PIPBUG ROM	
						4k		0FFF
0	0	X	X	1	X		SECOND BLOCK RAM	
							FIRST BLOCK RAM	
						3k	SECOND BLOCK RAM	
0	0	X	X	0	X		FIRST BLOCK RAM	0BFF
							PIPBUG ROM	07FF
						2k		06FF
0	0	X	X	1	X		SECOND BLOCK RAM	05FF
							FIRST BLOCK RAM	04FF
						1k	SECOND BLOCK RAM	03FF
0	0	X	X	0	X		FIRST BLOCK RAM	
							PIPBUG ROM	
						0		0000

NOTES: 1. * = Don't care for ROM and RAM; ** = Don't care for RAM. 2. Each block of RAM = 256 bytes.

Table 1 MEMORY MAP

ABC1500 LOGIC DIAGRAM

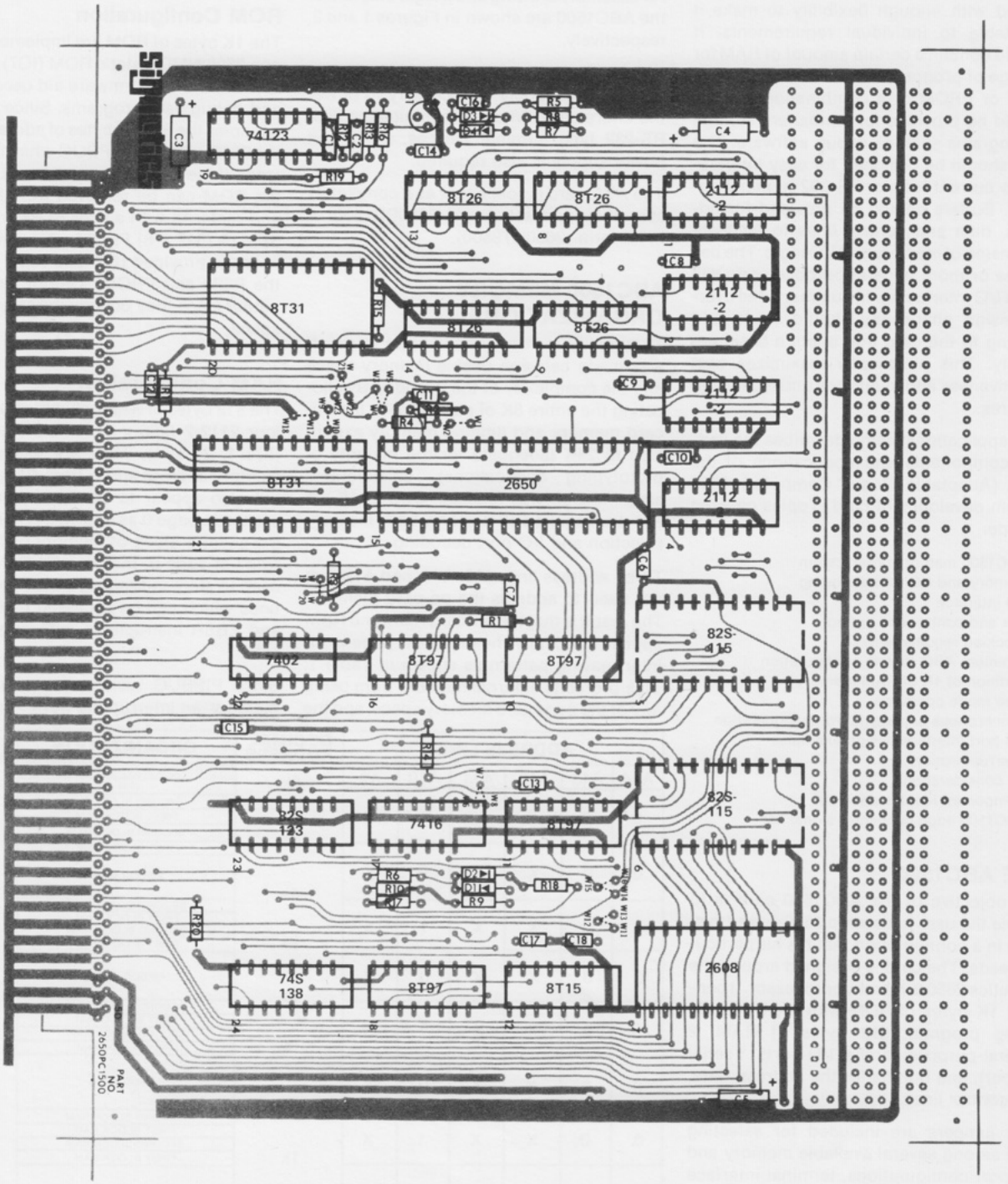


Figure 1

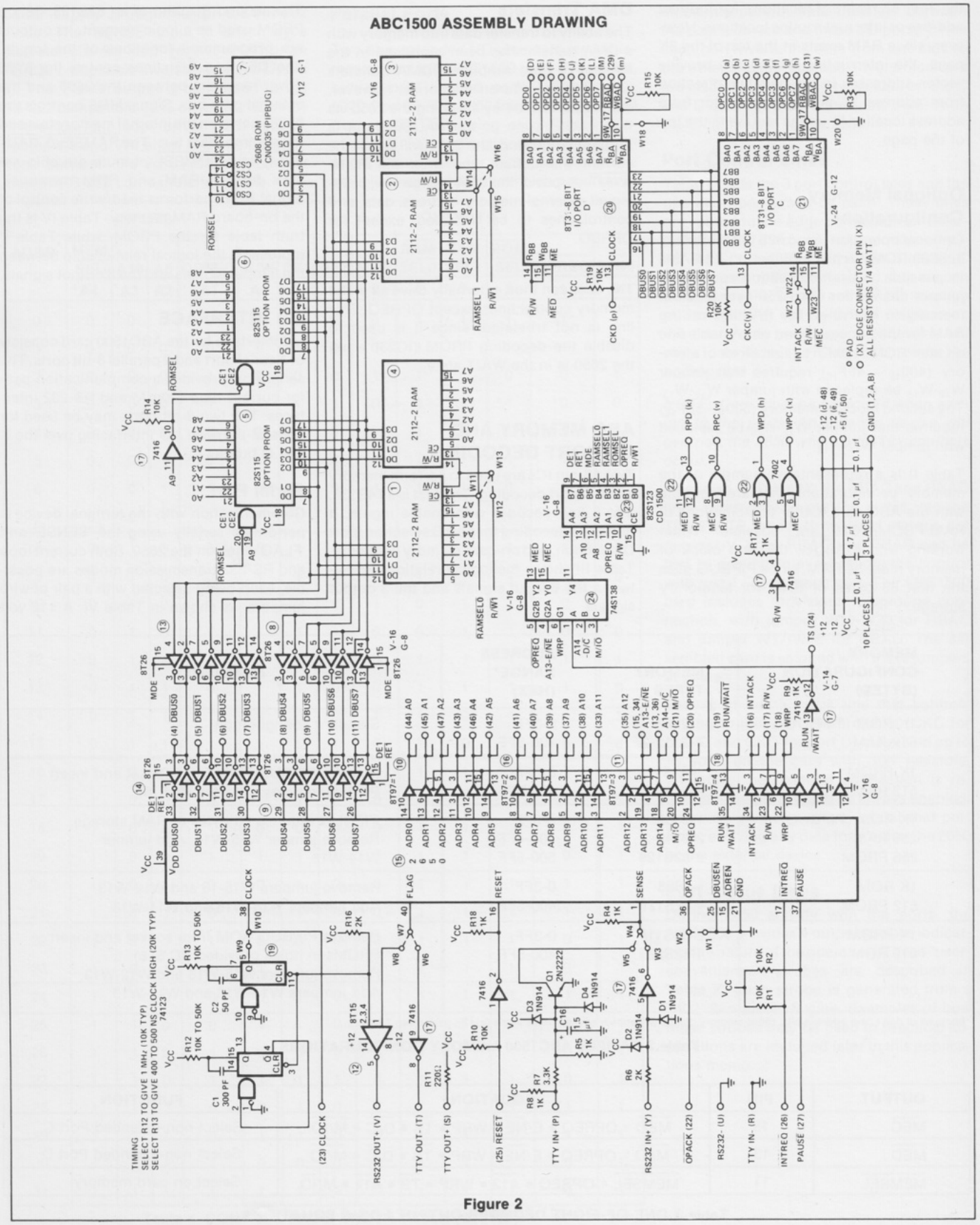

ABC1500 ASSEMBLY DRAWING
TIMING
SELECT R12 TO GIVE 1 MHz (10K TYP)
SELECT R13 TO GIVE 400 TO 500 NS CLOCK HIGH (20K TYP)
74123
R13 10K TO 50K
R12 10K TO 50K
C2 50 PF
C1 300 PF
CLR
CLOCK
(23) CLOCK
RS232 OUT+ (V)
TTY OUT- (T)
TTY OUT+ (S)
(25) RESET
TTY IN+ (P)
RS232 IN+ (Y)
OPACK (22)
RS232- (U)
TTY IN- (R)
INTREQ (26)
PAUSE (27)
ROMSEL
2608 ROM
CN0035 (PIPBUG)
8251S15
OPTION PROM
2112-2 RAM
RAMSEL1
RAMSEL0
R/W1
8T26
8T97
74S138
82S123
CD 1500
8T31-8 BIT
I/O PORT
C
D
CKD (p)
CKC(v)
INTACK
MED
MEC
MDE
OPREQ
RUN/WAIT
TS (24)
PAD
(X) EDGE CONNECTOR PIN (X)
ALL RESISTORS 1/4 WATT
10 PLACES
GND (1,2,A,B)

Figure 2

the first 63 memory locations for indirect address or interrupt routine locations. However, since RAM exists at the top of the 8K page, the interrupting device can provide vector addresses in the negative direction from address '0'. A negative vector from address location '0' wraps around to the top of the page.

Optional Memory Configurations

Optional operation using 82S129 PROMs or 82S229 ROMs in place of the 2112-2 RAMs is possible. This modification requires a jumper change for each 256-byte block of memory to exchange the R/$\overline{W}$ line on the RAM for the pin equivalent chip enable line on the PROM/ROM. The first block of memory (400_{16} - $4FF_{16}$) requires that jumper W_{12}-W_{13} be replaced with jumper W_{11}-W_{13}. The second block of memory (500_{16}-$5FF_{16}$) requires that jumper W_{15}-W_{16} be replaced with jumper W_{14}-W_{16}.

Table II is a representative sample of the memory configurations that are possible with the ABC card. Other combinations of RAM/PROM/ROM are possible. When working with PIPBUG, the first block of memory must be RAM, since PIPBUG uses the first 63 bytes of RAM for temporary storage.

DMA Transfers

The ability to transfer data into memory with a DMA transfer has been sacrificed in the interest of card simplicity. DMA transfers with external add-on memories, however, can be performed by stopping the 2650 via the 'PAUSE' line. If the $\overline{PAUSE}$ input is brought to ground, the 2650 will finish the current instruction, and then the RUN-/$\overline{WAIT}$ output of the 2650 will go low, causing all external memory address, data, and control lines to be tri-stated, except for OPREQ.

The user can then externally drive all of the memory control lines except OPREQ. This line is not tri-stated, since it is used to disable the decoding PROM (IC23) when the 2650 is in the WAIT state.

ABC MEMORY AND I/O PORT DECODING

Two 16-pin ICs are used to perform memory and I/O port decoding. The first is a 74S138, 3-to-8 line decoder with enable inputs. It performs decoding for port C selection, port D selection, and on-card memory decoding. Table III shows the logical relationship between the 6 input signals and the 3 output signals.

The second decoder is an 82S123, 32 x 8 PROM used as a logic element. Its outputs are programmed functions of the inputs. The DE1 and $\overline{RE1}$ lines control the 8T26 driver/receivers between the 2650 and the external data bus. Signal MDE controls the 8T26s between the internal memory bus and the external data bus. The $\overline{RAMSEL0}$, $\overline{RAMSEL1}$, and $\overline{ROMSEL}$ outputs are chip selects for the RAM and ROM memories. Signal R/$\overline{W1}$ performs read/write control of the on-board RAM memory. Table IV is the truth table for the PROM, while Table V represents the logical relationship between the 5 input signals and the 8 output signals.

I/O INTERFACE

I/O interface for the ABC1500 card consists of 1 serial port and 2 parallel 8-bit ports. The serial port provides a communication path for current loop (20mA) and RS-232 interfaces. The two 8-bit ports may be used for general-purpose I/O interfacing over the C and D buses.

Serial Port

Communication with the terminal device is performed serially using the 'SENSE' and 'FLAG' lines on the 2650. Both current loop and RS-232 transmission modes are possible, each being selected with a pair of wire jumpers, as shown in Table VI. A ±12 volt

MEMORY CONFIGURATION (BYTES)	MEMORY TYPES	ADDRESS RANGE* (HEX)	COMMENTS
1K ROM (PIPBUG) 512 RAM	1-2608 4-2112-2	0-3FF 400-5FF	Standard configuration
1K PROM 512 RAM	2-82S115 4-2112-2	0-3FF 400-5FF	Remove PIPBUG ROM from socket and insert PROMs in holes provided (IC5, 6).
1K ROM (PIPBUG) 256 RAM 256 PROM	1-2608 2-2112-2 2-82S129	0-3FF 400-4FF 500-5FF	PIPBUG requires 63 bytes of RAM storage. Remove jumper W15-W16. Add jumper W14-W16.
1K ROM 512 PROM	1-2608 4-82S129	0-3FF 400-5FF	Remove jumpers W15-16 and W12-W13. Add jumpers W14-W16 and W11-W13.
1K PROM 512 ROM	2-82S115 4-82S229	0-3FF 400-5FF	Remove PIPBUG ROM from socket and insert PROMs in holes provided (IC 5, 6). Remove jumpers W15-W16 and W12-W13. Add jumpers W14-W16 and W11-W13.

*Because of don't care address bits, these memory blocks will appear several times in the first 8K page (see Table I).

Table 2 SAMPLE ABC1500 MEMORY CONFIGURATIONS

OUTPUT	PIN	EQUATION	FUNCTION
$\overline{MEC}$	15	$\overline{MEC}$ = OPREQ • E/$\overline{NE}$ • WRP • $\overline{TS}$ • D/$\overline{C}$ • M/$\overline{IO}$	Select non-extended Port C
$\overline{MED}$	13	$\overline{MED}$ = OPREQ • E/$\overline{NE}$ • WRP • $\overline{TS}$ • D/$\overline{C}$ • M/$\overline{IO}$	Select non-extended Port D
$\overline{MEMSEL}$	11	$\overline{MEMSEL}$ = OPREQ • $\overline{A13}$ • WRP • $\overline{TS}$ • $\overline{A14}$ • M/$\overline{IO}$	Select on card memory

Table 3 ONE-OF-EIGHT DECODER OUTPUT LOGIC EQUATIONS

power supply is required for the RS-232 mode. The 'SENSE' input is driven by a discrete "current loop" receiver (Q1) or an RS-232 compatible inverter input (IC17, pin 5). The 'FLAG' output is connected to the RS-232 compatible 8T15 driver (IC12, pin 1) or the "current loop" driver (IC17, pin 9). Tables VII and VIII show the interconnections between the ABC1500 and current loop or RS-232 compatible terminals.

Parallel Ports

Two non-extended I/O channels are implemented on the ABC1500 with 8T31 8-bit, bidirectional latched ports (IC21-Port C, IC20-Port D). The 2650 transfers data to and from each port using single-byte, non-extended I/O instructions. Three control and 2 status lines for each port permit the establishment of a handshaking routine to efficiently control data transfers between the user's device and these I/O ports. Since each port inverts the data from one side to the other and the data bus drivers/receivers are also of the inverting type, data on the C and D buses will have the same polarity as the data internal to the 2650.

	INPUTS					OUTPUTS							
ADDR.	$\overline{\text{MEM SEL}}$	A10	A8	$\overline{\text{OPREQ}}$	$\overline{\text{R/W}}$	$\overline{\text{RE1}}$	DE1	MDE	$\overline{\text{RAM SEL0}}$	$\overline{\text{RAM SEL1}}$	$\overline{\text{ROM SEL}}$	$\overline{\text{OPREQ}}$	$\overline{\text{R/W1}}$
	A4	A3	A2	A1	A0	7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	0	0	1	1	1	1	1
1	0	0	0	0	1	1	0	0	1	1	1	1	0
2	0	0	0	1	0	0	0	1	1	1	0	0	1
3	0	0	0	1	1	1	1	0	1	1	1	0	0
4	0	0	1	0	0	1	0	0	1	1	1	1	1
5	0	0	1	0	1	1	0	0	1	1	1	1	0
6	0	0	1	1	0	0	0	1	1	1	0	0	1
7	0	0	1	1	1	1	1	0	1	1	1	0	0
8	0	1	0	0	0	1	0	0	1	1	1	1	1
9	0	1	0	0	1	1	0	0	1	1	1	1	0
10	0	1	0	1	0	0	0	1	0	1	1	0	1
11	0	1	0	1	1	1	1	0	0	1	1	0	0
12	0	1	1	0	0	1	0	0	1	1	1	1	1
13	0	1	1	0	1	1	0	0	1	1	1	1	0
14	0	1	1	1	0	0	0	1	1	0	1	0	1
15	0	1	1	1	1	1	1	0	1	0	1	0	0
16	1	0	0	0	0	1	0	0	1	1	1	1	1
17	1	0	0	0	1	1	0	0	1	1	1	1	1
18	1	0	0	1	0	0	0	0	1	1	1	0	1
19	1	0	0	1	1	1	1	0	1	1	1	0	1
20	1	0	1	0	0	1	0	0	1	1	1	1	1
21	1	0	1	0	1	1	0	0	1	1	1	1	1
22	1	0	1	1	0	0	0	0	1	1	1	0	1
23	1	0	1	1	1	1	1	0	1	1	1	0	1
24	1	1	0	0	0	1	0	0	1	1	1	1	1
25	1	1	0	0	1	1	0	0	1	1	1	1	1
26	1	1	0	1	0	0	0	0	1	1	1	0	1
27	1	1	0	1	1	1	1	0	1	1	1	0	1
28	1	1	1	0	0	1	0	0	1	1	1	1	1
29	1	1	1	0	1	1	0	0	1	1	1	1	1
30	1	1	1	1	0	0	0	0	1	1	1	0	1
31	1	1	1	1	1	1	1	0	1	1	1	0	1

Table 4 CONTROL PROM TRUTH TABLE (82S129)

Port Control Lines

Table IX lists the 3 port control lines and the operation performed by each. These lines are routed to the edge connector for external interface. If no external logic is connected, each port will be in the READ mode (C and D buses reflecting latched data in each port), since the $\overline{\text{WBAC}}$ and $\overline{\text{WBAD}}$ lines are pulled up to +5 volts with 10K resistors on the card. A low condition on either line will write data from the C or D bus into the appropriate port.

NOTE: Care must be exercised when writing to the ports. An external device will override the 2650 when "WRITE" conflicts occur.

As shown in Table IX, the $\overline{\text{RBAC}}$ and $\overline{\text{RBAD}}$ lines serve only to put the buses into the TRI-STATE mode. If the third state is not necessary, lines $\overline{\text{RBAC}}$ and $\overline{\text{RBAD}}$ can be tied to ground to allow read/write control with just 1 line on each port. The ABC1500 card includes provisions for ground connection, with jumper W19-W20 for $\overline{\text{RBAC}}$ and jumper W17-W18 for $\overline{\text{RBAD}}$. The assembled card is shipped with these jumpers in place.

Each port has a clock line that controls writing to that port. Both clocks (CKC for port C and CKD for port D) are pulled up to +5 volts on the card with 10K resistors. Therefore, no external connection is required if the ports are to be always enabled. A low on a clock line will inhibit that port from receiving any data from either the 2650 or the external device.

Port Status Lines

During 2650 activity with the ports, the ABC1500 provides 4 output strobes indicating the nature of the operation. These "user-convenience" strobes are described in Table X. Each strobe is generated from a 7402, 2-input NOR gate. Examples of how these strobes may be used in practical applications are included later in this applications memo.

OUTPUT	PIN	EQUATION	FUNCTION
DE1	9	DE1 = OPREQ • $\overline{R/W}$	Enables 2650 data bus drivers
$\overline{RE1}$	7	$\overline{RE1}$ = OPREQ • $\overline{R/W}$	Enables 2650 data bus receivers
MDE	6	MDE = OPREQ • MEMSEL • $\overline{\overline{R/W}}$	Select ABC1500 RAM, first block
$\overline{RAMSEL0}$	5	$\overline{RAMSEL0}$ = OPREQ • MEMSEL • A10 • $\overline{A8}$	Causes ABC1500 memory to drive data bus
$\overline{RAMSEL1}$	4	$\overline{RAMSEL1}$ = OPREQ • MEMSEL • A10 • A8	Select ABC1500 RAM, second block
$\overline{ROMSEL}$	3	$\overline{ROMSEL}$ = OPREQ • MEMSEL • $\overline{A10}$	Select ABC1500 ROM
$\overline{OPREQ}$	2	$\overline{OPREQ}$ = OPREQ	Invert OPREQ
R/$\overline{W1}$	1	R/$\overline{W1}$ = MEMSEL • $\overline{R/W}$	Read/write control for on-card RAM

Table 5 PROGRAMMED OUTPUT LOGIC EQUATIONS FOR THE 82S123 PROM

MODE OF TRANSMISSION	JUMPERS	POWER SUPPLY
20 Milliamp Current Loop	W6 - W7 W4 - W5	No Additional Supply Required
RS-232 Compatible	W7 - W8 W3 - W4	±12 Volt Supply

Table 6 SERIAL TRANSMISSION MODES

RS-232 STANDARD PIN NUMBER	ABC1500 PIN NUMBER	DESCRIPTION
1	N.C.	Protective Ground
2	Y	Transmitted Data (RS-232 IN+)
3	V	Received Data (RS-232 OUT+)
5	N.C.	Clear to send
6	N.C.	Data Ready
7	U	Signal Ground (RS-232 -)
8	N.C.	Received Line Signal Detector
20	N.C.	Data Terminal Ready

Table 7 RS-232C STANDARD CONNECTION

NOTE: N.C. = No Connection

The signals on pins 5, 6, 8, and 20 are used between data terminals and communication modems. Since the ABC1500 does not provide these "handshaking" lines, they should be tied together on the connector. In this way, the "Data Terminal Ready" line drives the other three lines to the proper state. Not all terminals, however, require this connection.

TELETYPE PIN NUMBER	ABC1500 PIN NUMBER	DESCRIPTION
6	T	Receiver - (TTY Serial OUT-)
7	S	Receiver + (TTY Serial OUT+)
3	R	Transmitter - (TTY Serial IN-)
4	P	Transmitter + (TTY Serial IN+)

Table 8 CURRENT LOOP CONNECTION

NOTE:

The teletype is normally a 20mA current loop type of receiver and a contact closure type of transmitter. The PIPBUG Debug program communicates with the teletype in a full-duplex mode, echoing characters as they are received.

PORT C CONTROL LINE TRUTH TABLE			
$\overline{WBAC}$	$\overline{RBAC}$	CKC	DESCRIPTION
1	0	X	External device reading port C
0	0	1	External device writing to port C
1	1	X	Tri-state C bus
X	X	0	Inhibit writing to port C from either external device or 2650

PORT D CONTROL LINE TRUTH TABLE			
$\overline{WBAD}$	$\overline{RBAD}$	CKD	DESCRIPTION
1	0	X	External device reading port D
0	0	1	External device writing to port D
1	1	X	Tri-state D bus
X	X	0	Inhibit writing to port D from either external device or 2650

Table 9 PORT CONTROL LINES

ABC GENERATED STATUS STROBE	DESCRIPTION
WPC	Positive true pulse, high for the duration of WRP, indicating that the 2650 is placing data into port C.
WPD	Positive true pulse, high for the duration of WRP, indicating that the 2650 is placing data into port D.
RPC	Positive true pulse, high for the duration of OPREQ, indicating that the 2650 is reading port C.
RPD	Positive true pulse, high for the duration of OPREQ, indicating that the 2650 is reading port D.

Table 10 ABC GENERATED CONVENIENCE STROBES

BUS AND CONTROL LINE BUFFERS

The 2650 data bus is buffered with two 8T26 tri-state inverting driver/receivers with a 40mA current sink capability (IC9, 14). Logic on the card consumes approximately 1mA, leaving a net external drive capability of 39mA. When the 2650 is not transferring data over the bus, these buffers are in the tri-state mode. The output of the buffers ($\overline{DBUS0}$-$\overline{DBUS7}$) is routed to the edge connector (pins 4-11).

The on-board memory bus is buffered from the external data bus with two 8T26s (IC8, 13). These buffers are never in the tri-state mode. When not actively transferring data, these devices are reading the external data bus to the internal memory bus. Double buffering between the memory and 2650 allows data polarity to be preserved.

The 2650 address bus and control lines are buffered with four 8T97 hex tri-state buffers (IC10, 11, 16, 18). The state of the TS control line (IC17, pin 12) determines whether the drivers are in the tri-state mode or actively driving the external lines. When the 2650 is in the RUN mode, the TS line is low, enabling the 8T97s to be in the active state. When the 2650 is in the WAIT mode, the TS line is high, and the address bus drivers are in the high-impedance state. External control of the TS line can change the address bus drivers to the active mode when the 2650 is in the WAIT state, but cannot force the drivers to the high-impedance state when the 2650 is "running."

The external drive capability of the address bus is essentially the same as the drive capability of the 8T97 (48mA sink capability). The control lines will be loaded slightly by logic on the card. The maximum load is on the A13•E/$\overline{NE}$ and A14•D/$\overline{C}$ lines. Card logic will consume 2mA of the 48mA capability.

ABC1500 CLOCKING REQUIREMENTS

The clock on the ABC1500 card is implemented with a 74123 (IC19) dual monostable multivibrator. One half of the 74123 is connected in an astable mode to determine the frequency of the clock. The other half is connected as a one-shot to set the pulse width.

When running under PIPBUG, the 2650 requires a 1MHz clock for serial communication with the TTY. The PIPBUG program performs all formatting for the 110 baud interface and uses the clock as a timing base. The stability requirements of the clock are not critical, and the one-shot configuration is adequate. For KT9500 assembly, it may be necessary to select frequency resistor R12 to insure the 1MHz operation and the sampling of each bit at its approximate midpoint. R12 is typically 7.5K. In most cases pulse width resistor R13 will be fixed at 20K to obtain a clock high time between 400 and 500ns.

An external clock may be used in place of the one-shot configuration. When using an external clock, jumper W9-W10 must be removed, and the external clock can then be applied to pin 23 on the edge connector.

A MINIMUM ABC1500 SYSTEM CONFIGURATION

In Figure 3, the ABC1500 card is interfaced with 3 other components to configure a basic prototyping system.

The reset switch is used to reset the 2650's Instruction Address Register (IAR) to zero and to enter the PIPBUG program. This negative true input is inverted by IC17 to obtain the positive true polarity required by the 2650.

BASIC PROTOTYPING SYSTEM

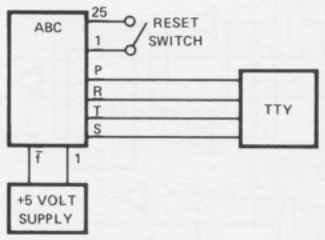


Figure 3

ADDITION OF 1K OF RAM MEMORY TO THE ABC1500 CARD

It is possible to expand the memory of the ABC1500 card by using the wire-wrap area. In the example shown in Figure 4, 12 ICs are used to add 1K of RAM memory.

The memory occupies the last 1K section of page 3 and uses a single N7430 gate to decode the appropriate signals. These signals can be obtained from wire wrap pins inserted into the appropriate holes on the card.

The 8T26 buffers are used to multiplex the single input and output from each memory (1K x 1) onto the external data bus. When

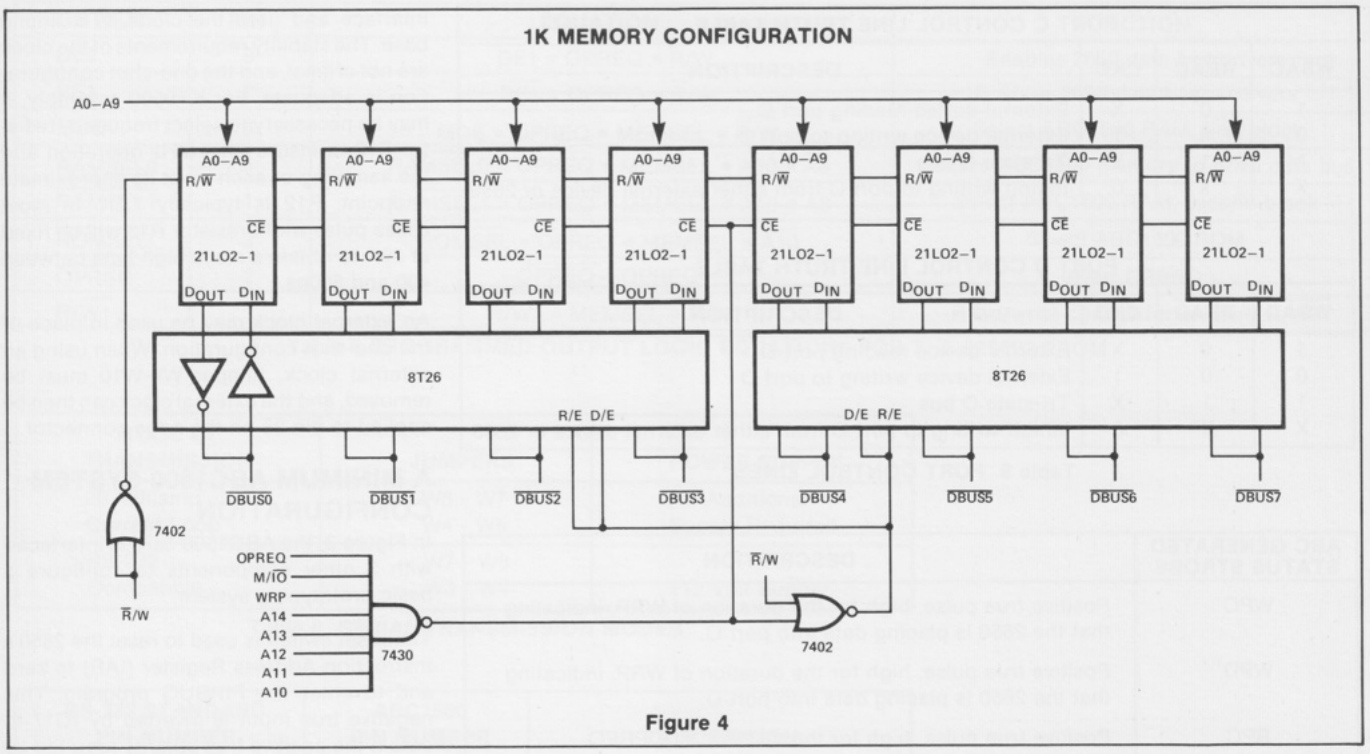


Figure 4

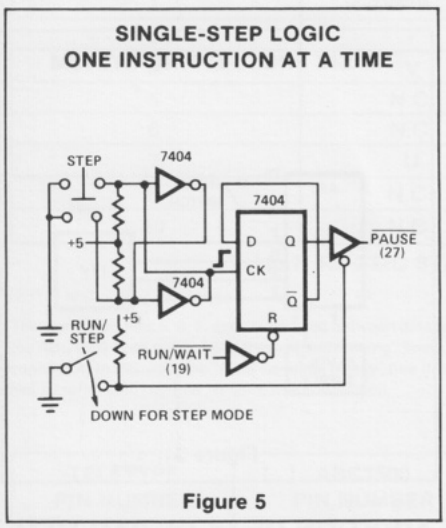


Figure 5

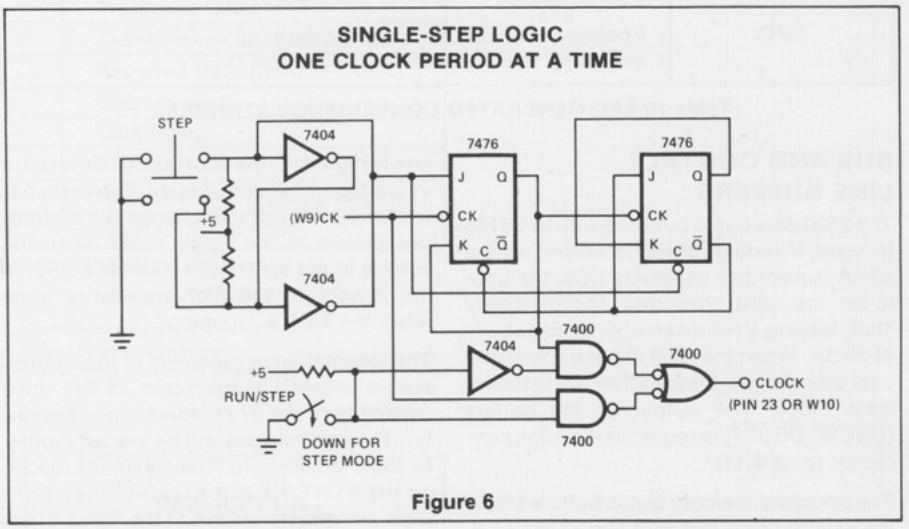


Figure 6

not communicating with the memory, the buffers are reading the external data bus.

STEP MODE OPERATION

The ability to cycle through a program one step at a time is very useful when checking out software. The 2650 microprocessor is ideally suited for this type of operation because of its static design. An example of the logic necessary to put the ABC1500 card into the step mode for single-instruction execution is shown in Figure 5.

To enter the step mode, the RUN/STEP switch is depressed. This enables the tri-state driver tied to the pause input on the card (pin 27), and immediately causes the $\overline{\text{PAUSE}}$ line of the 2650 to go true or low, since the Q output of the D flip-flop is low for the RUN mode. De-bounce logic is not necessary, since the 2650 will eventually recognize the low condition on the $\overline{\text{PAUSE}}$ line after executing any number of RUN /$\overline{\text{WAIT}}$ cycles.

When the 2650 enters the WAIT state, the RUN/$\overline{\text{WAIT}}$ line (pin 19) goes low, allowing the flip-flop to be clocked to the SET state (Q goes high) when the momentary contact STEP switch is depressed. With the Q output of the flip-flop high, the $\overline{\text{PAUSE}}$ line will go high taking the 2650 out of the WAIT state. When the 2650 enters the RUN mode, the flip-flop will be reset, and the $\overline{\text{PAUSE}}$ line will again go true, forcing the 2650 into the WAIT state after completing one instruction. This procedure is repeated for each depression of the switch.

It is also possible to step through a program 1 clock period at a time. This procedure is

useful for observing the status of the bus and control lines during each instruction cycle. In this case, instead of pausing the 2650, the clock is controlled with the logic shown in Figure 6.

To work in this mode, the clock jumper W9-W10 is removed and a wire is connected from W9 to the clock input on the first J-K flip-flop in Figure 6, and to one of the inputs on the 2-input NAND gate. When in the RUN mode, the RUN/STEP switch is up, enabling this NAND gate to control the ORing NAND gate. The ORing NAND gate is fed to the clock pin on the ABC card or to W10. This completes a path between the output of the one-shot on the card and the clock input on the 2650.

To enter the step mode, the RUN/STEP switch is depressed. This blocks the clock between W9 and W10. The JK configuration then synchronizes the asynchronous step input with the clock to produce a pulse 1 clock period wide for each depression of the momentary contact STEP switch. This allows 1 clock pulse to be provided to the 2650 for executing instructions 1 clock period at a time.

One approach that can be used for displaying the data and address bus during the single clock period mode is seen in Figure 7. Here the address bus is displayed with an LED and current limiting resistor added to each line. External latches are not required since the 2650 holds the current address state when the clock is low.

To display the data bus will require that the bus be latched, since the bus will be tri-stated when OPREQ is low. One of the ports (Port D in Figure 7) can be used for data storage if that port is not needed by the software. Here the external data bus ($\overline{DBUS0}$-$\overline{DBUS7}$) is connected to the port bus with LEDs and current limiting resistors on each line. The port READ/WRITE line is controlled by the OPREQ line through an external inverter. When OPREQ is high, the port is being written into from the data bus. When OPREQ is low, the data is latched in the port which is now in the READ mode.

SYNCHRONOUS/ASYNCHRONOUS OPERATION

The operation acknowledge ($\overline{OPACK}$) input to the 2650 indicates completion of an external operation. This allows for asynchronous control of external devices. The assembled card is configured to work synchronously, with $\overline{OPACK}$ grounded by jumper W2-W1. This requires input data to be returned to the processor in 850ns or less at a cycle time of 2.4μs. If this timing constraint is too severe, asynchronous operation can be en-

ADDRESS AND DATA BUS DISPLAY

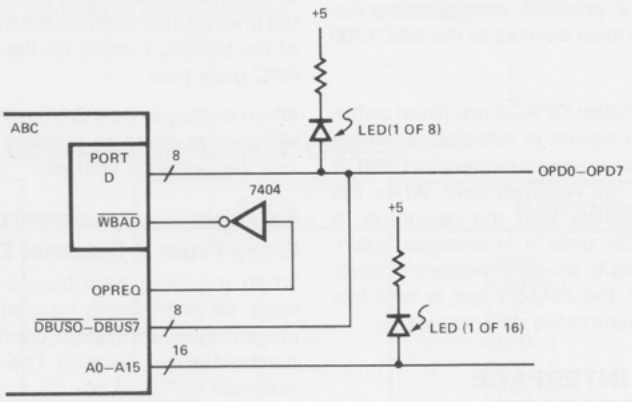


Figure 7

ASYNCHRONOUS OPERATION USING OPACK

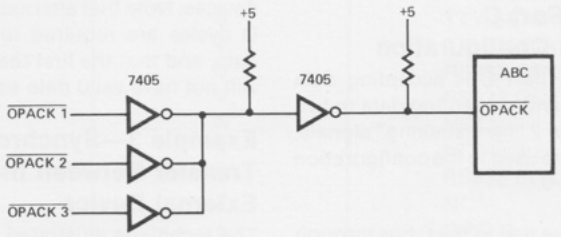


Figure 8

I/O LOGIC TO PORT C

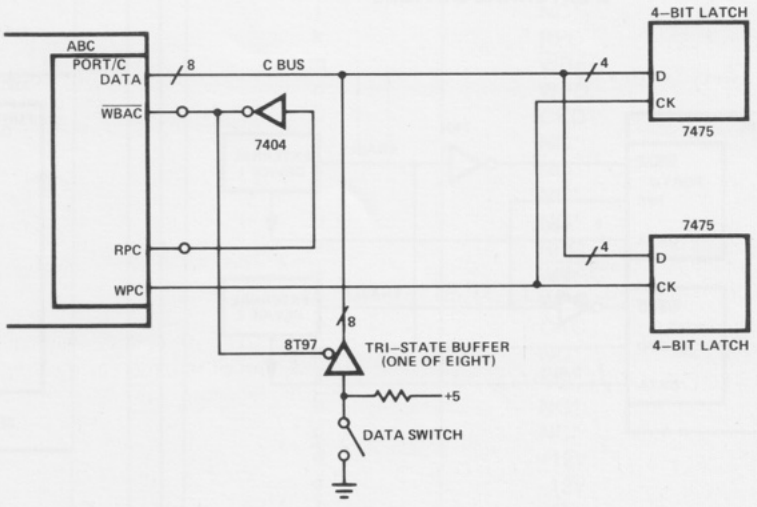


Figure 9

abled by removing the jumper and driving the $\overline{\text{OPACK}}$ line (pin 22).

Figure 8 is a possible configuration for connecting 3 slow devices to the ABC1500 card.

This scheme holds $\overline{\text{OPACK}}$ low (true) until a slow external device is selected, at which time the device drives its respective $\overline{\text{OPACK}}$ line high for the required time. When the device is finished with the operation, it lowers $\overline{\text{OPACK}}$ until it is selected again. When transfers to on-card memory or ports are executed, the $\overline{\text{OPACK}}$ line is held low (true) for synchronous data transfers.

I/O PORT INTERFACE DESIGN EXAMPLES

"Handshaking" signals are provided to simplify communication between the ports and the user's device. Several examples are presented to illustrate possible interface techniques for connecting the 2 ports to external devices.

Example 1—Port C Input/Output Configuration

In this example, port C is accepting data from 8 switches and presenting data to two 4-bit latches. The 2 "handshaking" signals, RPC and WPC, are used in the configuration shown in Figure 9.

The 8 switches are tied to the C bus through tri-state buffers. Input write control line $\overline{\text{WBAC}}$ is controlled by an inverter with its input tied to RPC. When the 2650 performs a read from port C (REDC), line RPC goes true forcing $\overline{\text{WBAC}}$ low and allowing port C to store data from the C bus. The output of the inverter also controls the tri-state enable of the buffers, turning on the buffers when RPC goes true.

When writing to port C from the 2650, WPC will go true, clocking the data on the C bus into the two 4-bit latches.

Example 2—Synchronizing Data Entry From 2 External Devices

When inputting data from 2 external devices, an interleaving transfer scheme can prevent synchronization conflicts between the devices and the 2650. The configuration is shown in Figure 10.

External device 1 places data onto the C bus and clocks it into port C when the 2650 is reading port D. Likewise, external device 2 places data onto the D bus and clocks it into port D when the 2650 is reading port C, thus preventing conflicts between 2650 activity and loading of the ports from the external devices. Note that alternate read C and read D cycles are required to read the proper data, and that the first read cycle executed will not have valid data associated with it.

Example 3—Synchronizing Data Transfer Between the 2650 and an External Device

The technique illustrated in Figure 11 may be used when transferring data asynchronously between the 2650 and an external device.

In this example, a D latch is used to synchronize data transfers from the 2650 to an external device. When the 2650 loads port C, handshake signal WPC goes true, clocking the D latch to the SET state. The Q output of the latch is tied to the 'SENSE' input (pin Y with jumper W3-W4 in). The 2650 can be programmed to monitor the 'SENSE' line. For the 'SENSE' line HIGH, the program will loop in a WAIT state. When the device has accepted the data, it will reset the latch and force the 'SENSE' line to zero. The 2650 can then place new data in the port.

INTERRUPT OPTION

When responding to an interrupt, the 2650 obtains the interrupt vector by reading the data lines when INTACK is issued. The state of the control lines is such that a read of port C would also be performed (ADR13•E/$\overline{\text{NE}}$ and ADR14•D/$\overline{\text{C}}$ are both low). To prevent a conflict between the interrupting device and port C on the card, the INTACK signal is fed to port C to disable the port during interrupts. For certain applications, however, it may be desirable to use port C to input the vector address. This optional operation may be obtained by replacing the W21-W22 jumper with a jumper between W22-W23.

KIT CONSTRUCTION

Kit construction is straightforward requiring only wire, wire cutters, and a soldering iron. Each component has a number which is stamped on the PC card in white. The component number also identifies the location of pin 1 for an IC. The component identification list identifies each number

SYNCHRONOUS DATA ENTRY FROM 2 EXTERNAL DEVICES

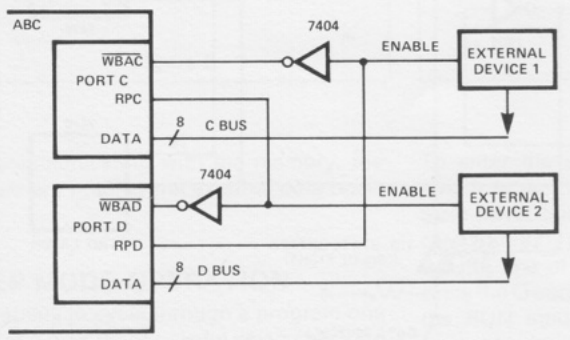


Figure 10

PORT C OUTPUT SYNCHRONIZATION LOGIC

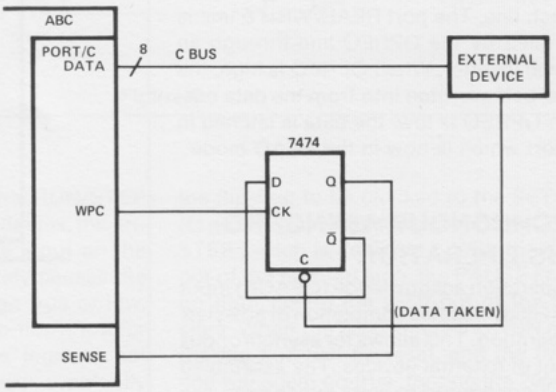


Figure 11

with the appropriate component. Sockets are provided for the 2650 and for the 2608 PIPBUG ROM. If the user expects to use the RAM/PROM/PROM option (see Section 3), he may want to insert sockets in the RAM holes. Reference should be made to Section 7 for resistor values for the one-shot clock configuration. The kit is shipped with values of 7.5K for R12 and 20K for R13, but it may be necessary to increase or decrease these values to obtain 1MHz operation. Also, if it is desirable to change the relative position of the RAM and ROM in page zero, the 82S129 control PROM can be re-programmed at the user's discretion.

ABC 1500 EDGE CONNECTOR SIGNAL LIST

PIN #	FUNCTION
1	GND
2	GND
3	NC*
4	$\overline{\text{DBUS0}}$
5	$\overline{\text{DBUS1}}$
6	$\overline{\text{DBUS2}}$
7	$\overline{\text{DBUS3}}$
8	$\overline{\text{DBUS4}}$
9	$\overline{\text{DBUS5}}$
10	$\overline{\text{DBUS6}}$
11	$\overline{\text{DBUS7}}$
12	NC*
13	A14—D/$\overline{\text{C}}$
14	NC*
15	A13—E/$\overline{\text{NE}}$
16	INTACK
17	R/W
18	WRP
19	RUN/$\overline{\text{WAIT}}$
20	OPREQ
21	M/IO
22	$\overline{\text{OPACK}}$
23	CLOCK
24	$\overline{\text{TS}}$
25	$\overline{\text{RESET}}$
26	$\overline{\text{INTREQ}}$
27	$\overline{\text{PAUSE}}$
28	NC*
29	RBAD
30	NC*
31	RBAC
32	NC*
33	AII
34	A13—E/$\overline{\text{NE}}$
35	A12
36	A14—D/$\overline{\text{C}}$
37	A9
38	A10
39	A8
40	A7
41	A6
42	A5
43	A3
44	A0
45	A1
46	A4
47	A2
48	+12V
49	-12V
50	+5V

PIN #	FUNCTION
A	GND
B	GND
C	NC*
D	OPD 0
E	OPD 1
F	OPD 2
H	OPD 3
J	OPD 4
K	OPD 5
L	OPD 6
M	OPD 7
N	NC*
P	TTY SERIAL IN +
R	TTY SERIAL IN -
S	TTY SERIAL OUT +
T	TTY SERIAL OUT -
U	RS232 GROUND
V	RS232 OUTPUT
W	NC*
X	NC*
Y	RS232 INPUT
Z	NC*
a	OPC 0
b	OPC 1
c	OPC 2
d	OPC 3
e	OPC 4
f	OPC 5
g	OPC 6
h	OPC 7
j	NC*
k	RPD
m	$\overline{\text{WBAD}}$
n	WPD
p	CKD
r	NC*
s	NC*
t	NC*
u	NC*
v	RPC
w	$\overline{\text{WBAC}}$
x	WPC
y	CKC
z	NC*
$\bar{a}$	NC*
$\bar{b}$	NC*
$\bar{c}$	NC*
$\bar{d}$	+12V
$\bar{e}$	-12V
$\bar{f}$	+5V

*NC = No Connection

ABC 1500 COMPONENT IDENTIFICATION LIST

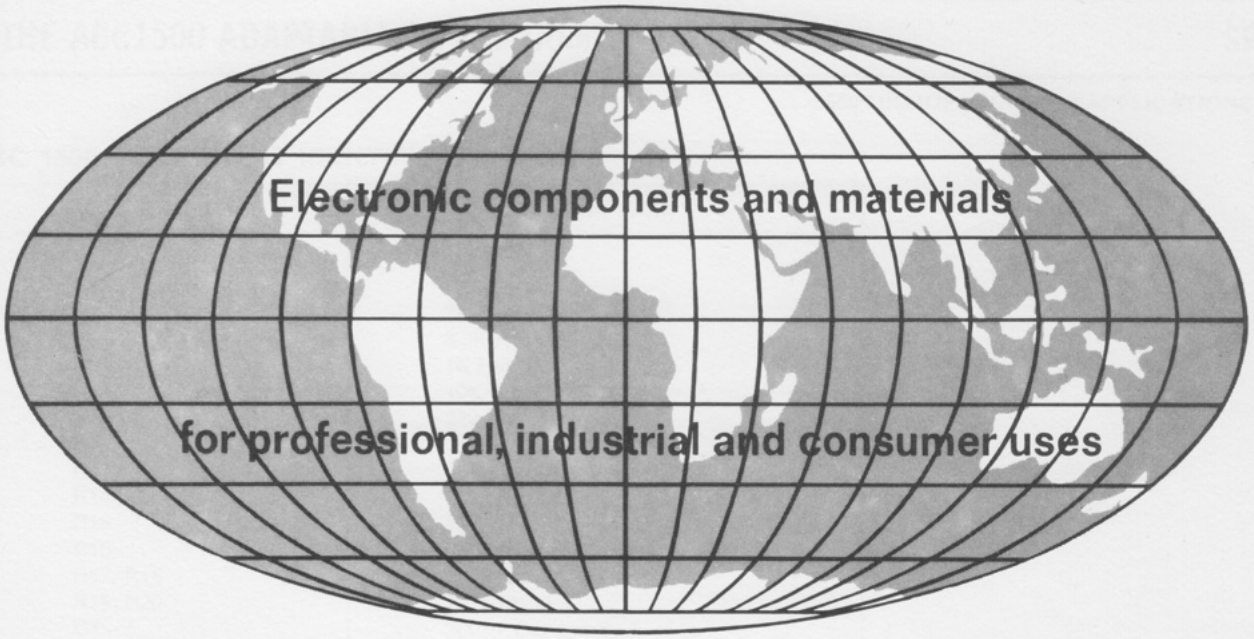
COMPONENT*	DESCRIPTION**
R1, R2, R3	10K Resistor
R4, R5	1K Resistor
R6	2K Resistor
R7	3.3K Resistor
R8, R9	1K Resistor
R10	10K Resistor
R11	220-ohm Resistor
R12	7.5K (typical) Resistor
R13	20K (typical) Resistor
R14	1K Resistor
R15	10K Resistor
R16	2K Resistor
R17, R18	1K Resistor
R19, R20	10K Resistor
C1	300PF Capacitor
C2	50PF Capacitor
C3, C4, C5	4.7μf Capacitor, Tan. 50 DC
C6-C15, C17, C18	0.1μf Capacitor, Ceramic
C16	1.5μf Capacitor, Tan. 20 DC
D1, D2, D3, D4	1N914 Diode
Q1	2N2222 Transistor
1,2,3,4	2112-2 RAM
5,6	82S115 PROM (optional)
7	2608 ROM (socket)
8,9	8T26 Tri-State Driver/Receiver
10,11	8T97 Tri-State Driver
12	8T15 RS232 Driver
13,14	8T26
15	2650 Microprocessor (socket)
16	8T97
17	N7416 Hex Inverter Buffer
18	8T97
19	N74123 Monostable Multivibrator
20,21	8T31 I/O Port
22	N7402 Quad 2-Input NOR
23	82S123 PROM
24	N74S138 3- to 8-line Decoder

* All IC component numbers are located on card at pin 1 of IC.

** All resistors ¼ watt.

Signetics 2650 Microprocessor application memos currently available:

AS50	Serial Input/Output
AS51	Bit and Byte Testing Procedures
AS52	General Delay Routines
AS53	Binary Arithmetic Routines
AS54	Conversion Routines
SP50	2650 Evaluation Printed Circuit Board Level System (PC1001)
SP51	2650 Demo Systems
SP52	Support Software for use with NCSS Timesharing System
SP53	Simulator, Version 1.2
SP54	Support Software for use with the General Electric Mark III Timesharing System
SP55	The ABC1500 Adaptable Board Computer
SS50	PIPBUG
SS51	Absolute Object Format (Revision 1)
MP51	2650 Initialization
MP52	Low Cost Clock Generator Circuits
MP53	Address and Data Bus Interfacing Techniques
MP54	2650 Input/Output Structures and Interfaces



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